R16

Code No: 134AK

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, April - 2018
COMPUTER ORGANIZATION
(Common to CSE, IT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a)	Explain RTL and its control function.	[2]
b)	Compare horizontal and vertical organization.	[3]
c)	Differentiate jump and loop instructions.	[2]
d)	Briefly explain special processor activities.	[3]
e)	What is an assembler?	[2]
f)	Explain the machine code for: LES DI,[0600H] and NEG 50[BP].	[3]
g)	Explain overflow and underflow.	[2]
h)	Differentiate isolated I/O and memory mapped I/O.	[3]
i)	Explain the cache incoherence.	[2]
j)	Explain the locality of reference.	[3]

PART-B

(50 Marks)

2.a) List and explain different performance measures used to represent a computer system performance.
b) Elucidate the functioning of a Micro program sequencer. [5+5]

OR

3.a) Elucidate common bus system.
b) Formulate a mapping procedure that provides eight consecutive micro instructions for each routine. The operation code has 7 bits and control memory has 4096 words. [5+5]

4.a) Explain the register organization in 8086.
b) Elucidate machine language instruction formats. [5+5]

OR

5.a) Explain the pin configuration details of 8086.
b) Explain the assembler directives with examples. [5+5]

6.a) Explain the steps involved in writing a program using an assembler.
b) Write a program to find out the number of positive numbers and negative numbers from a given series of signed numbers. [5+5]

OR

7.a) Add the contents of the memory location 4000H:0600H to contents of 5000H:0700H and store the result in 8000H:0900H
b) Write a program for addition of two numbers. [5+5]

8.a) Draw a flow chart for Floating point Add/subtract operations.
b) Illustrate asynchronous communication interface in detail. [5+5]

OR

9.a) Explain in detail with neat sketch Booth Multiplication Algorithm.
b) Explain different types of modes of control. [5+5]

10.a) Explain arithmetic pipeline with example.
b) Elucidate Inter processor communication. [5+5]

OR

11.a) Elucidate array processor in detail.
b) Explain various Interconnection Structures. [5+5]

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PART – A

(25 Marks)

1.a)	What is the purpose of BUN instruction?	[2]
b)	Define computer organization, computer architecture.	[3]
c)	Contrast 8086 minimum mode with maximum mode.	[2]
d)	How an address is latched in 8086?	[3]
e)	What is the need of a linker?	[2]
f)	What is the difference between a macro and a procedure?	[3]
g)	What is the disadvantage of strobe method?	[2]
h)	Provide the hardware for signed-2's complement addition and subtraction.	[3]
i)	Define miss penalty for cache memory.	[2]
j)	Draw the system bus structure for multiprocessors.	[3]

PART – B

(50 Marks)

2. List the registers for the basic computer and give their functionality in program execution. [10]

OR

3. Describe the micro programmed control organization and compare its advantages over hardwired control. [10]

4. Evaluate the following arithmetic statement using zero, one, two and three address instructions. Use the conventional symbols and instructions.
X = (A+B) * (C+D). [10]

OR

5. Does 8086 support instruction pipelining? Justify your answer with relevant example instructions. [10]

6. Develop an assembly language program to find out numbers odd and even numbers in a given series of 16-bit hexa decimal numbers. [10]

OR

7. Elaborate on the techniques used to pass parameters to procedures in assembly language program. [10]

8. Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied. (+33) × (-12). [10]

OR

9. Design a circuit for a 4 × 4 First In First Out Buffer and explain its functionality. [10]

10. A digital computer has a memory unit of 64K * 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of 4 words.
(a) How many bits are there in the tag, index, block and word fields of the address format?
(b) How many bits are there in each word of cache and how are they divided into function? Include a valid bit. [10]

OR

11. Does pipelining get affected by data dependencies among the instruction? Justify your answer with lucid examples. [10]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, December - 2018
COMPUTER ORGANIZATION
(Common to CSE, IT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a) Write the generic Instruction types present in a computer system. [2]
b) What is the difference between a direct and an indirect address instruction? [3]
c) List the four basic functions of the CPU. [2]
d) Give a note on Instruction Set of 8086. [3]
e) What is an interrupt service routine in microprocessor? [2]
f) How a clock signal is generated in 8086 microprocessor? [3]
g) List four peripherals devices that produce an acceptable output for a person to understand. [2]
h) How many characters per second can be transmitted over a 1200 baud line in Synchronous serial transmission? [3]
i) What are the difficulties that cause the instruction pipeline to deviate from its normal operation? [2]
j) Draw the structure of general purpose multicomputer. [3]

PART - B

5 × 10 marks = 50

2.a) How many references to memory are needed for each type of instruction to bring an operand into a processor register? Explain.
b) With the help of a block diagram, explain how do we select the address of control memory. [5+5]

OR

3.a) Give a brief note on instruction cycle.
b) List and explain the functional units of a computer. [5+5]

4. Draw and explain the 8086 Processor Architecture. [10]

OR

5.a) Explain the Assembler Directives**.**
b) Discuss the Physical memory organization. [5+5]

6. How to pass parameters to procedures in 8086? Explain in detail with an ALP**.** [10]

OR

7.a) Is ‘c’ an assembly language? Justify your answer.
b) With an assembly language program explain stack organization in 8086. [4+6]

8. Compare interrupt driven data transfer scheme with DMA. Using block diagram explain interrupt driven transfer scheme. [10]

OR

9. Explain Booths multiplication algorithm with example. [10]

10.a) Distinguish between the virtual memory and cache memory. Write the merits and demerits of virtual memory.

b) Give a neat sketch that illustrates the components in a typical memory hierarchy. [5+5]

OR

11.a) With the help of a neat diagram explain the match logic for one word of associative memory.

b) What are the various forms available for establishing an interconnection network in a multi processor system? [5+5]

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PART – A

(25 Marks)

1.a) Define computer. Specify the different types of computers. [2]
b) Draw the Block diagram of Digital Computer. [3]
c) How is the addressing mode of an instruction communicated to the CPU? [2]
d) Write a short note on Machine language instruction formats. [3]
e) What is the role of stack in calling a subroutine and returning from the routine? [2]
f) Define a macro SQUARE that calculates the square of a number. [3]
g) Determine the base of the numbers in each case for the following operations to be correct: 14/2 = 5. [2]
h) How the floating-point numbers are represented and used in digital arithmetic operations? [3]
i) Sometimes processors in tightly coupled multiprocessor environment will be idle. Why? [2]
j) Differentiate between a conventional scalar processor and a vector processor. [3]

PART – B

(50 Marks)

2. Explain the generic Instruction types present in a computer system. [10]

OR

3.a) Compare and Contrast the Computer Design and Computer Architecture.
b) Compare hardwired control with microprogrammed control. [5+5]

4. Elaborate of the Instruction set of 8086. [10]

OR

5. Discuss the physical address formation in different addressing modes. [10]

6. Write an assembly language program to construct a 4 digital decimal number to its binary equivalent, using a procedure for dividing a number by two. [10]

OR

7. Explain interrupt cycle of 8086 and demonstrate interrupt programming. [10]

8. Explain the floating point addition- subtraction unit with a neat diagram. [10]

OR

9. Compare interrupt driven data transfer scheme with DMA. Using block diagram explain interrupt driven transfer scheme. [10]

10.a) Draw a space time diagram for six segment pipeline showing the time it takes to process eight tasks.

b) Consider the multiplication of two 40×40 matrices using a vector processor.
i) How many product terms are there in each inner product and how many inner products must be evaluated?
ii) How many multiply add operations are needed to calculate the product matrix? [5+5]

OR

11.a) Explain the parallel processing architecture and its uses.

b) With the help of a neat diagram explain the match logic for one word of associative memory. [5+5]

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